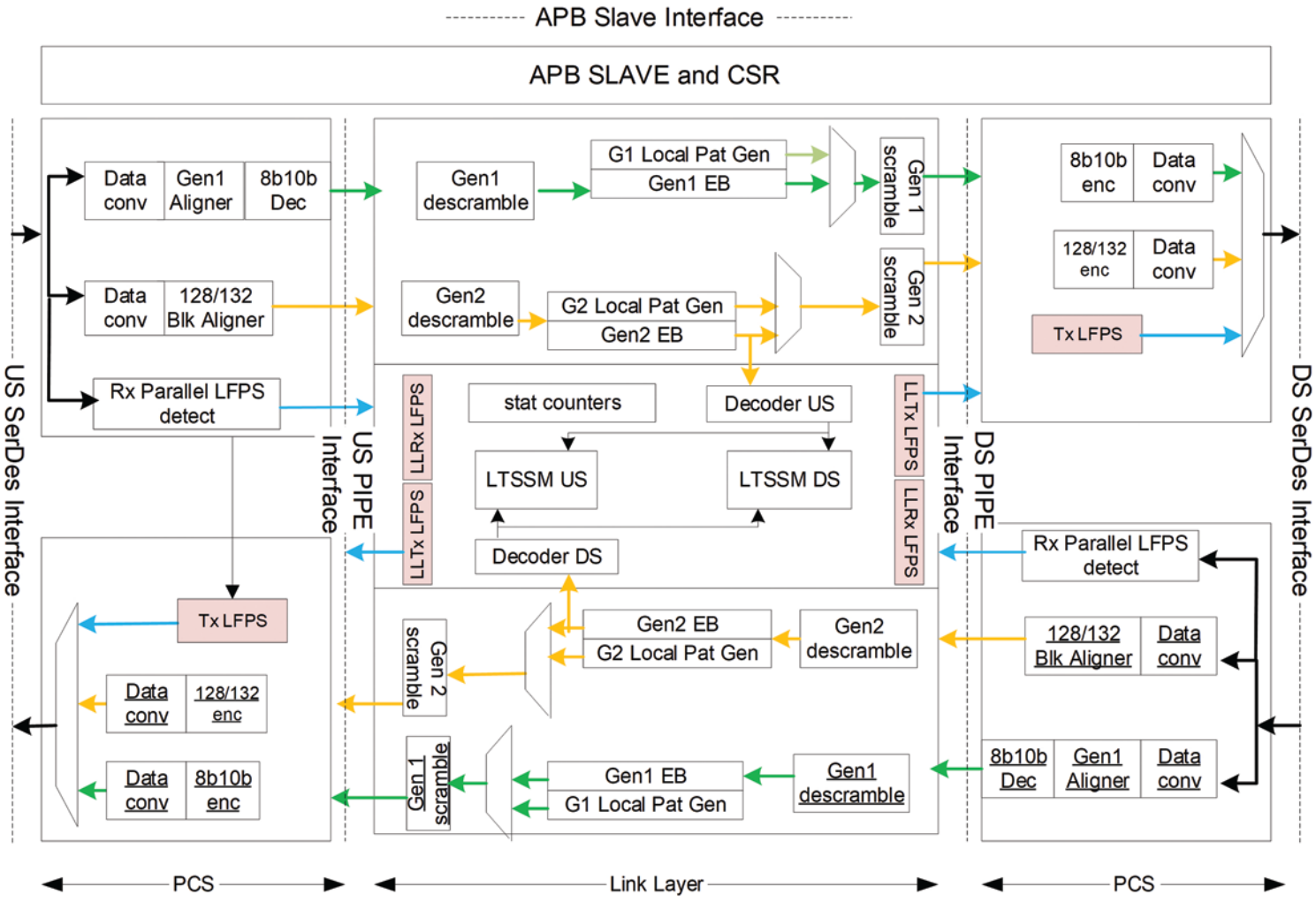
USB3.1 Retimer Controller IP Core

Overview

OpenFive introduces USB3.1 Retimer IP core for host captive, device captive and active cable applications. It is compliant to USB3.1 standard's Appendix E and USB3.2 standard except dual lane support. The IP core supports Gen1 (5Gbps) and Gen2 (10Gbps) speeds. It supports optional USB3.1 PIPE interfaces for seamless integration with standard PHY. Alternatively, it supports 20/32bit generic SerDes interface and APB 32bit interface. The core offers CSR to enhance debug and configuration capability.

Block Diagram



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Key Features

- Compliant to USB3.1 Appendix E standard
- Supports Gen 1(5G) and Gen2(10G) speeds
- Supports all low power states
- Supports MCU CSR interface to drive ASIC Control and Status Register
- Supports PCS logic with 8b/10b for Gen1 and 128b/132b for Gen2
- Supports generic SerDes interface
- Optional support to external PHY with PIPE interface
- SRIS architecture
- "Pass through" and "Local loopback" supported
- Provision to monitor key events including internal errors
- Provision to monitor link states
- Option to tune PIPE control signal through CSR interface
- Master loopback support for production test
- Option to generate LFPS pattern in debug mode
- Support for Internal and External loopback modes and SerDes testability using test pattern

Deliverables

- Synthesizable Verilog RTL source code
- SystemVerilog based verification environment including device and host models
- SystemVerilog based comprehensive testsuite
- User Guide
- Lint, CDC and synthesis scrips
- FPGA constraint file