



POWER VIA IMPROVEMENT SCRIPT

Thimma Raju Vadde

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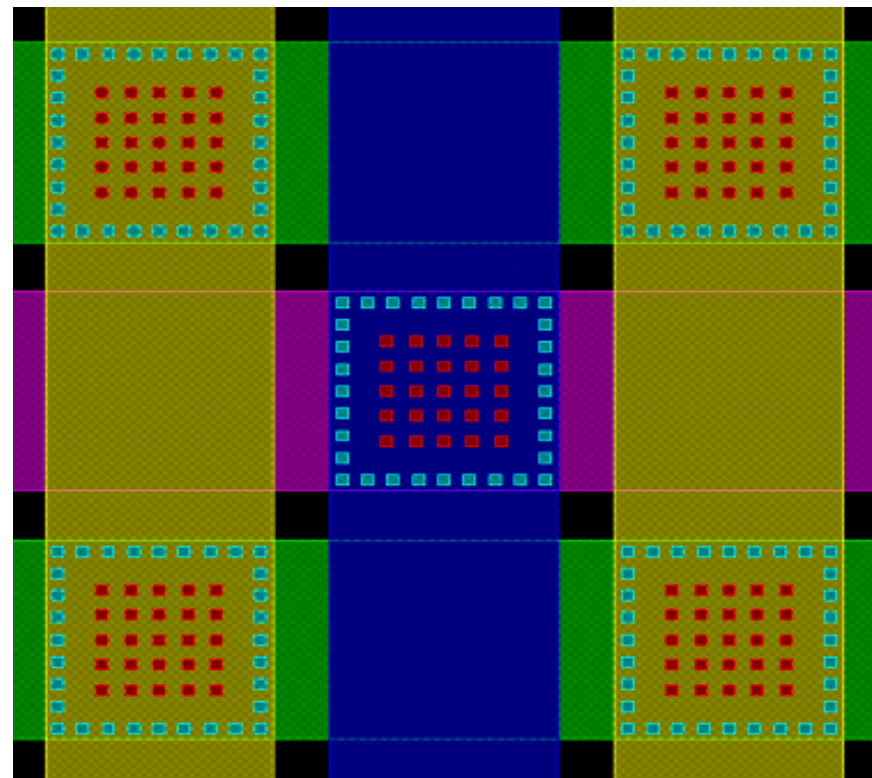
Agenda

- **Introduction to power via improvement flow using Calibre script**
- **Why this script is needed and scope of it**
- **Demonstration and analysis**



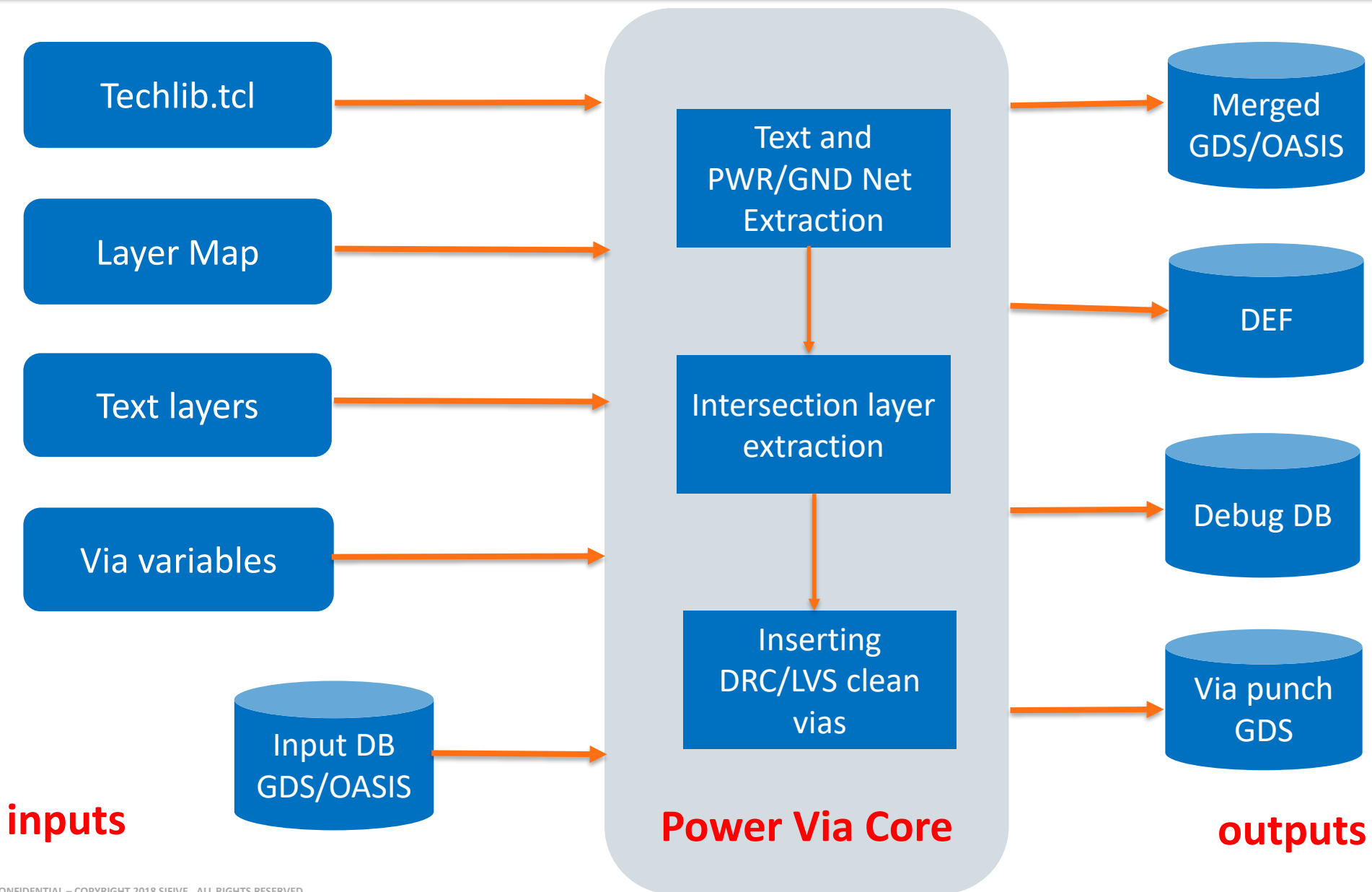
Introduction

- **Power via flow inserts VIA to reduce IR and EM drops in chip design.**
- **Calibre power via flow doesn't disturb connectivity or cause new DRC's.**



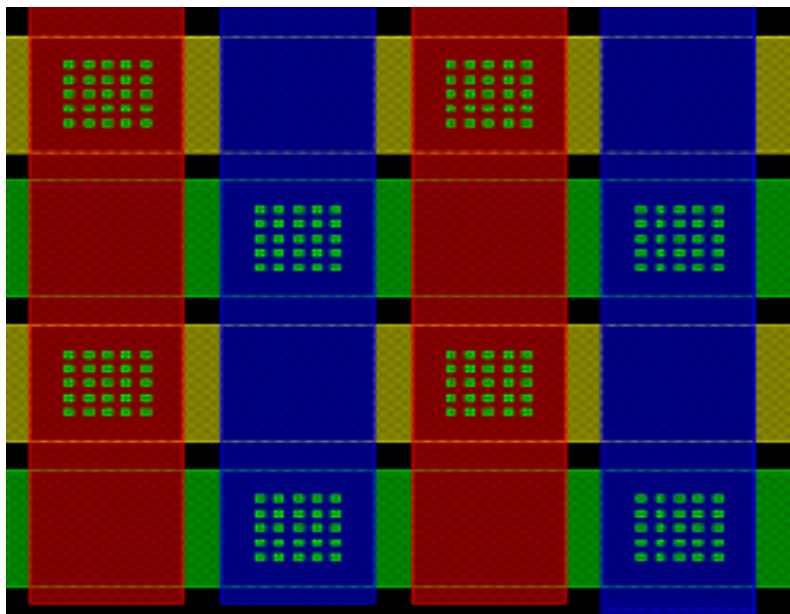


Power Via Flow

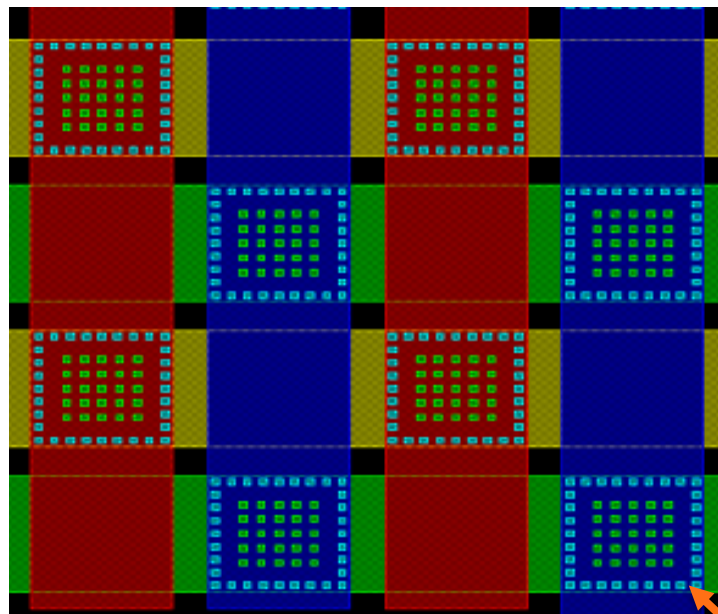




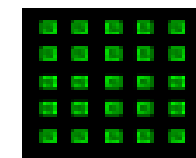
Sample design flow



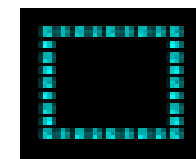
initial DB



improved DB



original vias



inserted vias

inserted vias



Run Results

- **Outputs**
 - merged DB (GDS/OASIS)
 - via_punch_fill.gds (new vias DB added by power via flow)
 - incremental.def
 - net_aware_PWR_GND.oas (Debug DB)
- **Runtime is less than an hour for top level block with 16 CPU's.**
- **Vias that are added by power via flow**



```
RULECHECK VIA1iCFILLR_count ..... TOTAL Result Count = 166218
RULECHECK VIA2iCFILLR_count ..... TOTAL Result Count = 224830
RULECHECK VIA3iCFILLR_count ..... TOTAL Result Count = 15450
RULECHECK VIA4iCFILLR_count ..... TOTAL Result Count = 88874
RULECHECK VIA5iCFILLR_count ..... TOTAL Result Count = 297270
RULECHECK VIA6iCFILLR_count ..... TOTAL Result Count = 382236
RULECHECK VIA7iCFILLR_count ..... TOTAL Result Count = 547592
RULECHECK VIA8iCFILLR_count ..... TOTAL Result Count = 553888
RULECHECK VIA9iCFILLR_count ..... TOTAL Result Count = 857
RULECHECK VIA10iCFILLR_count ..... TOTAL Result Count = 1692920
```



Debug DB

- Debug DB : `net_aware_PWR_GND.oas`
- We can identify original and added vias by analyzing layers in the debug DB.

- Original metal layers

182		original_M11_rule
183		original_M02_rule

- Original via layers

144		VIA11_rule
145		VIA11BAR_rule

- Metal layers identified by flow for each net

1		M11_VDD_rule
3		M11_VS8_rule
13		M02_VDD_rule
15		M02_VS8_rule

- same net metal layer intersection

172		M11_M02_intersection_rule
173		M02_M03_intersection_rule

- Fill area for each via layer

193		VIA11_fillarea_rule
194		VIA02_fillarea_rule

- Exclusion layer for metals/vias

161		M11EXCL_rule
162		M02EXCL_rule

- Inserted vias

12321		VIA11CFILLR_count
12322		VIA02CFILLR_count
12323		VIA03CFILLR_count



Thanks!