OpenFive 100G PCS IP Core

Overview

The OpenFive 100G PCS supports PCS/PMA termination for 100GE, 50GE, 40GE, 25GE and 10GE ports in compliance with 802.3 specifications. Figure 1 shows a high-level diagram of the 100G PCS IP core. On the system side, a configurable media independent interface provides connection to OpenFive's 100G MAC/RS IP module, to support the 100GE (CGMII), 50GE (50GMII), 40GE (XLGMII), 25GE (25GMII), and 10GE (XGMII) rates. On the line side, a parallel interface provides direct connection to third-party 4x 25G NRZ and/or 2x 50G PAM4 SERDES modules. Different bus width (compile-time) options are provided to support both ASIC and FPGA implementations.

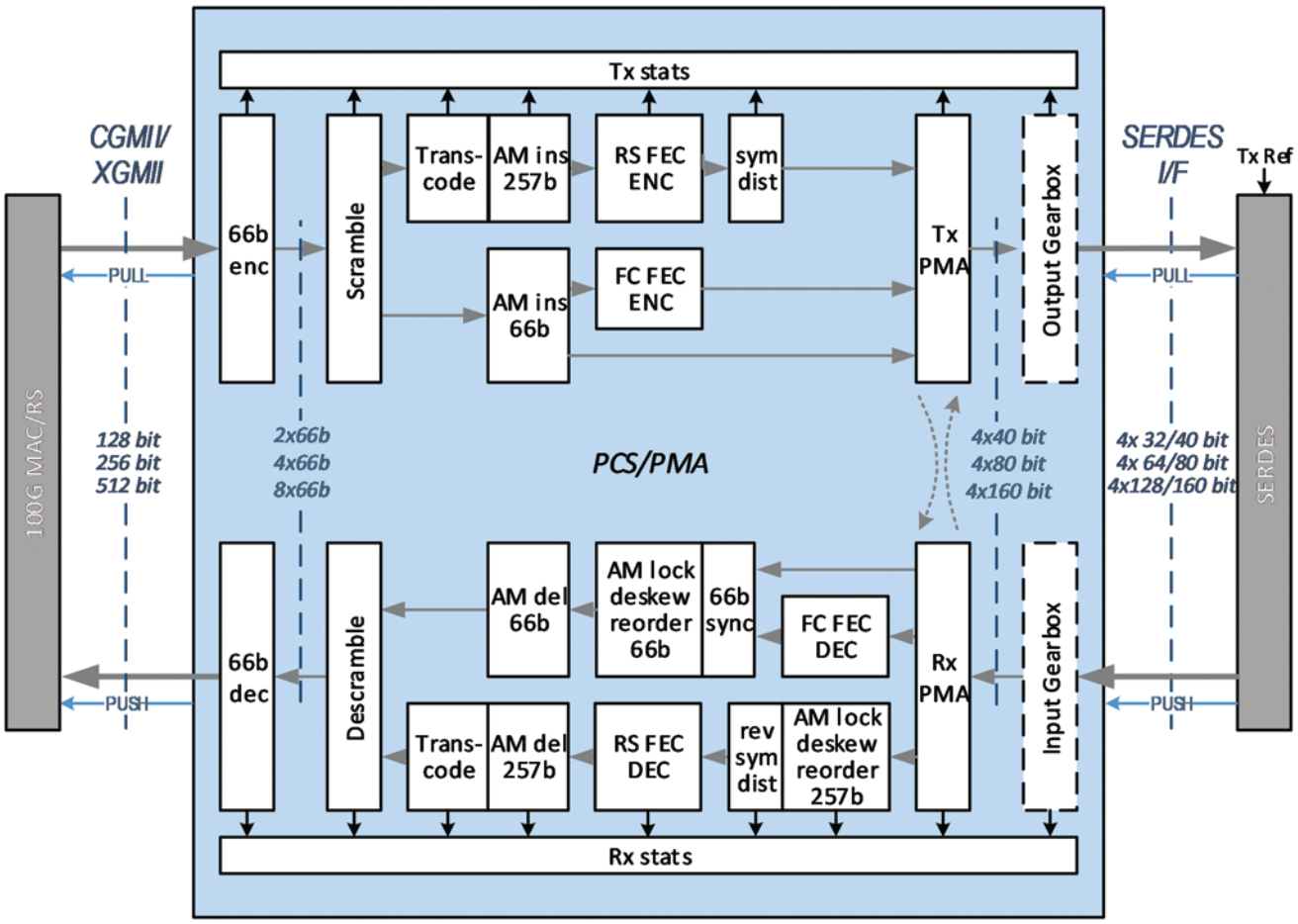

Figure 1 – 100G PCS/PMA functional diagram

The 100G PCS/PMA module implements the 802.3 PCS and PMA sublayers to support 100GE, 50GE, 40GE, 25GE and 10GE Ethernet PHYs based on the 66b encoding (per clauses 82, 133, 107, 49), the KR FEC (per clauses 91 and 108), the KP FEC (per clauses 91 and 134), and the BASE-R/Fire Code FEC (per clause 74).

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Features

- Single channel PCS/PMA for 100GE, 50GE, 40GE, 25GE and 10GE Ethernet ports.
- Compile-time bus width options to support ASIC and FPGA implementations.
- Compile-time and run-time configuration options to support PCS and PMA termination for Ethernet PHYs based on the 66b encoding (clauses 82/133/107/49), the BASE-R/Fire Code FEC (clause 74), the KR FEC (clauses 91/108), the KP FEC (clauses 91/134), and the Consortium LL-FEC.

Media independent interface

- A flexible CGMII/XGMII port, providing seamless connection to OSi's 100G MAC/RS IP module.
- Supports CGMII/XLGMII (clause 81), 50GMII (clause 132), 25GMII (clause 106) and XGMII (clause 46) operation modes.

SerDes interface

- SerDes parallel interface options for 25G NRZ lanes, 50G PAM4 lanes, and future 100G PAM4 lanes.

BASE-R processing

- 66b block lock, AM lock/deskew/reorder, AM insertion/deletion and scrambling for Ethernet ports based on the 66b and Fire Code FEC encodings.
- Per-lane programmable markers.
- Automatic consequent actions.
- Scrambled Idle Test pattern, Hi BER detection.
- Lock alarms, HiBER alarm, BIP statistics.

Fire Code FEC

- Compliant with 802.3 clause 74, for the support of 100GE/40GE/25GE/10GE cable and backplane PHYs.
- Optional 66b block error marking.
- Corrected/uncorrected block counters.

Reed Solomon FEC

- Compliant with 802.3 clauses 91, 134, and 108, for the support of 100GE/50GE/25GE optical, cable and backplane PHYs.
  - RS10(544,514, t=15) KP FEC.
  - RS10(528,514, t=7) KR FEC.
- Compliant with the Consortium low latency FEC (LL-FEC) for 25GE.
  - RS10(272, 257+1, t=7).
- Transcoding, scrambling and alignment marker insertion/deletion (programmable markers).
- AM lock/deskew/reorder of four 25G FEC lanes (100GE) or two 25G FEC lanes (50GE).
- Symbol distribution.
- FEC degrade functionality for 100GE and 50GE.
- Optional error indication functionality (for 66b sync header corruption), and optional error monitoring (>K errors every 8k codewords).
- Alarms and monitoring counters (e.g. symbol errors, corrected/uncorrected codewords, etc.).

PMA

- Compliant with 802.3 clauses 83, 135, 109 and 51.
- Test pattern generation for NRZ's PRBS31, PRBS9 and square-wave, and PAM4's PRBS31Q, PRBS13Q and SSPRQ.
- Remote and local loopbacks.

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