MCMR FEC (Forward Error Correction) IP Core

Multi-Channel Multi-Rate FEC IP

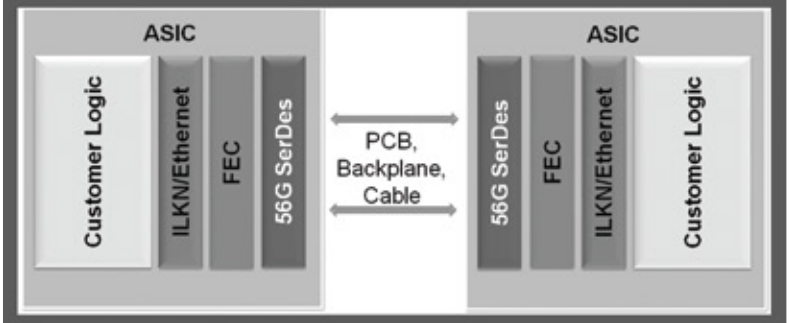
OpenFive's MCMR FEC IP core is a single solution to meet the requirements of different protocols like Interlaken, Flex Ethernet, and 802.3x to significantly improve bandwidth by enabling high speed SerDes integration. The FEC can easily achieve a BER (Bit Error Rate) of $<10^{-15}$ with an input BER of $>10^{-6}$, which is required by most electrical interface standards using high speed SerDes.

Built upon a flexible and robust architecture, OpenFive's MCMR FEC IP core is compatible with various SerDes supporting different widths. The MCMR FEC IP supports bandwidth up to 400G with the ability to connect 32 SerDes lanes.

Features

- Supports up to 56Gbps SerDes
- Supports bandwidth up to 400G
- Support for KP4 RS (544,514) & KR4 RS (528,514)
- Supports Interlaken, Flex Ethernet & 802.3x protocols
- Supports configurable alignment marker
- PRBS test pattern generator and loopback test

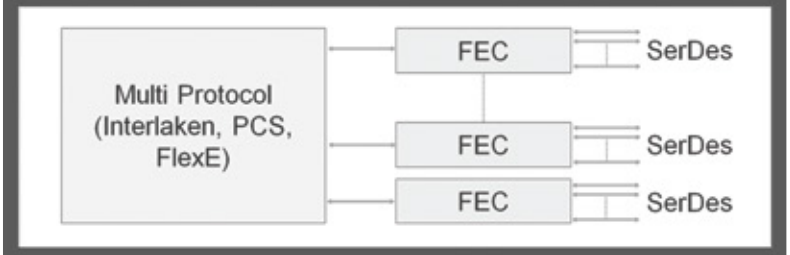
The block diagram on right shows the functional representation of how the FEC relates to the protocol layer and the SerDes lanes. As an example, a single MCMR FEC can be used to interface with up to 32 SerDes lanes with an aggregate bandwidth of up to 400G. Likewise, to achieve a 1.2Tbps bandwidth with 24 lanes 50G SerDes interface, you would need three instances of MCMR FEC IP.



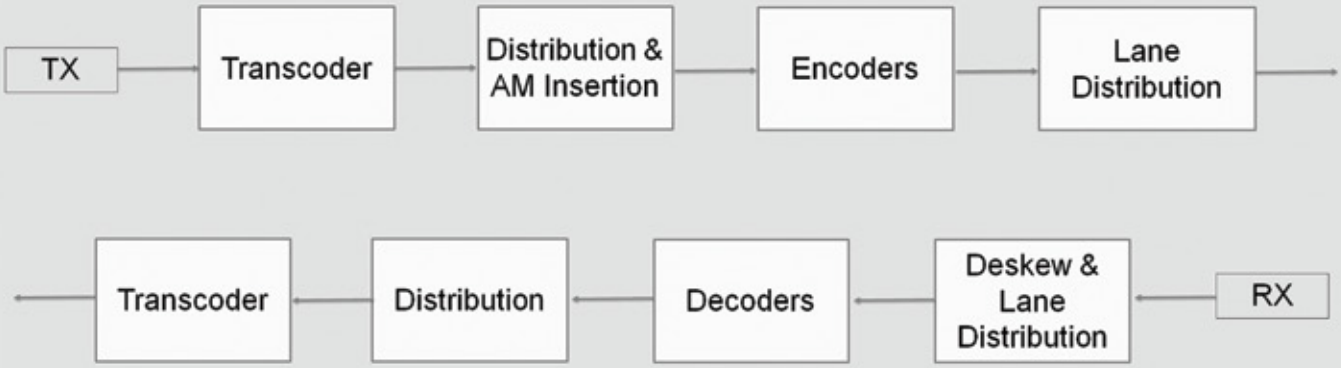
OpenFive MCMR FEC IP

OpenFive's MCMR FEC IP core supports the Interlaken standard specification and the Ethernet standard specification.

Designed and tested to be easily synthesizable into many ASIC technologies, the OpenFive MCMR FEC IP core is uniquely built to work with off-the-shelf SerDes from leading technology vendors. Using vendor-specific proven SerDes allows for fast and seamless integration of the MCMR FEC IP core into the technology of choice.



Functional Block Diagram



FEC IP Block Diagram

MCMR FEC (Forward Error Correction) IP Core

Applications

- Packet Processing/NPU
- Traffic Management
- Switch Fabric
- Switch Fabric Interface
- Framer/Mapper
- FPGA etc.

Deliverables

OpenFive's MCMR FEC IP is shipped with the following deliverables:

- Synthesizable RTL
- Template CAD scripts for synthesis and static timing
- Assertions for the user interface and config registers
- Sanity test simulation environment
- RX/TX BFMs
- Documentation:
- SiFive IP Specification
- Memory-Mapped Register Manual
- Design Verification Plan