OpenFive 100G MAC IP Core

Overview

OpenFive 100G MAC IP core supports MAC/RS termination for 100GE, 50GE, 40GE, 25GE, 10GE, 5GE, 2.5GE and 1GE in compliance with 802.3 specifications. Figure 1 shows a high-level diagram of the 100G MAC IP core.

On the system side, the user interface provides connection to the customer-side packet buffers. The user I/F provides sideband signals for packet delineation, packet error, link status, and Ethernet flow control indications. Customer-specific equest-response delays are tolerated using a FIFO.

On the line side, three separate xMII interfaces are provided for connection to specific PCS/PMA modules: a flexible CGMII/XGMII port, for connection to OSi's 100G PCS/PMA companion module, an XGMII port, for connection to a third-party 25/10/5/2.5GE PCS/PMA module, and a GMII port, for connection to a third-party 1GE PCS/PMA module.

Compile-time bus width options are provided to support both ASIC and FPGA implementations.

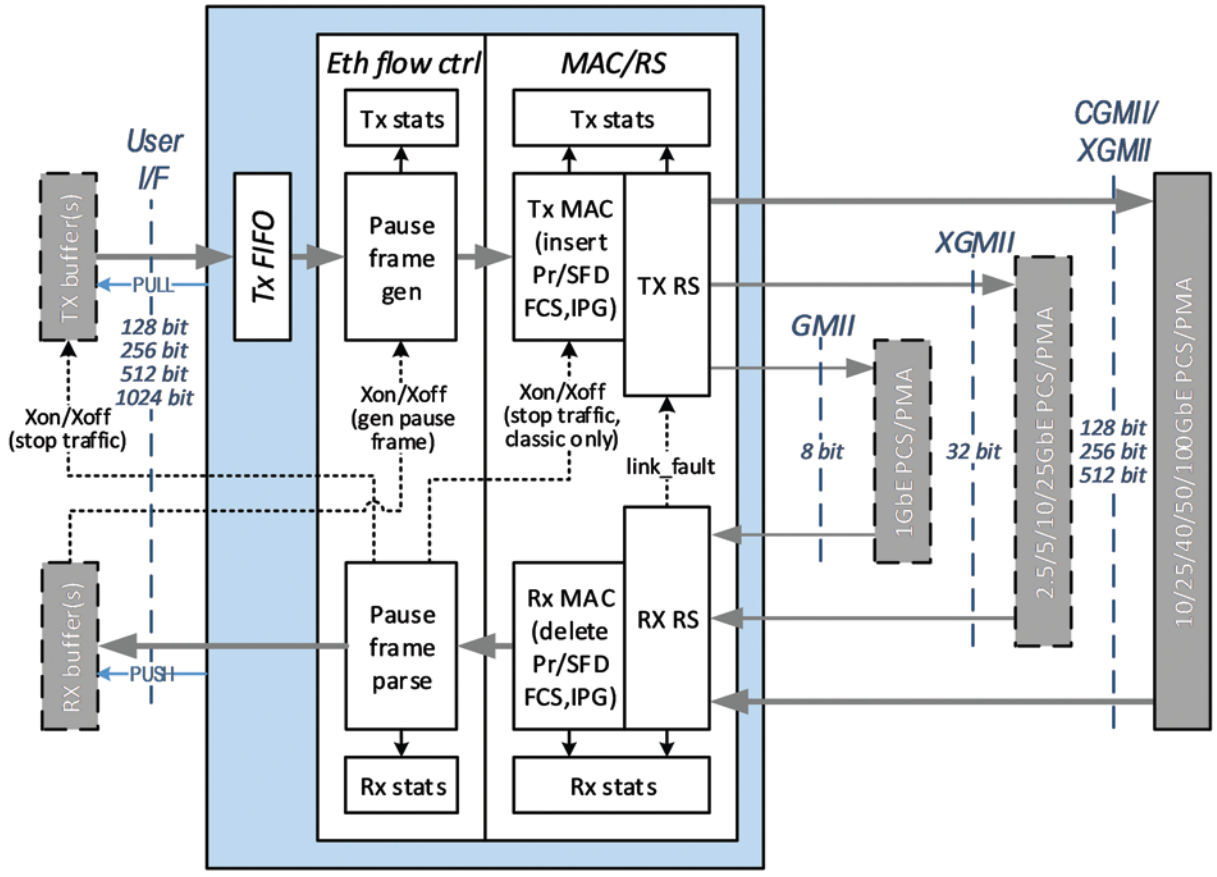

Figure 1 – 100G MAC/RS functional diagram

The 100G MAC terminates the MAC and RS sublayers, inserting/deleting the Preamble/SFD, FCS and IPG fields, generating/terminating the control characters used to delineate the packets and encode explicit fault indications, and adapting the packet stream to/from the active media independent interface. The 100G MAC supports both classic (802.1x) and class-based (802.1Qbb) Ethernet flow control. Pause frames are generated, using the configured Pause quanta values. The received Pause frames are detected by correctly matching the DA, EtherType and Opcode fields.

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Features

- Single channel MAC/RS for 100GE, 50GE, 40GE, 25GE, 10GE, 5GE, 2.5GE and 1GE MAC ports.
- Compile-time bus width options to support both ASIC and FPGA implementations.
- Optional classic (802.3x) and priority-based flow control (802.1Qbb).
- MAC layer processing, including full statistics (IEEE 802.3, IETF RFC 2665 MIB/MIB-II and RFC 2819 RMON counters), in both transmit and receive directions.
- Supports VLAN tagged frames (IEEE 802.1Q) and double-tagged frames (QinQ).
- OAM, LACP, BPDU frame detection.
- Non-pause control frames optionally dropped.
- All frames are subject to configurable minimum and maximum frame length checks.
- Preamble/SFD and FCS are deleted/inserted or bypassed to/from the user interface.
- Option to overwrite SA on transmitted frames.
- Option to drop received frames that do not match configured DA.
- Option to filter packets that do not match.
- FCS checking and generation.
- Supports padding of small (<64 byte) frames.
- Interpacket gap generation based on Deficit Idle Counter (100/50/25/10/5G/2.5GE) or using a fixed length (1GE).
- Link status automatic consequent actions (LF→RF, RF→Idle reflections).
- Compliant with 802.3 clause 78 (802.3az standard) for Energy Efficient Ethernet (EEE).

User interface

- Simple user (MAC service) interface, consists of a single segment of 128, 256, 512 or 1024 bits.
- Input/output sideband signals to control/ indicate packet delineation, packet errors, Ethernet link status, and Ethernet flow control.
- Tolerates arbitrary request-response delays on the transmit direction.

Media independent interface

Three separate media independent interfaces provide connection to specific PCS/PMA modules:

- A CGMII/XGMII port, for connection to OpenFive's 100GE, 50GE, 40GE, 25GE and 10GE PCS/PMA module, to implement PHYs based on 66b (clauses 82/133/107/49), KR FEC (clauses 91/108), KP FEC (clauses 91/134), and Fire Code FEC (clause 74).
- An XGMII port, for connection to a third-party 25/10G/5/2.5GE PCS/PMA module (e.g. 25GBASE-T).
- An GMII for connection to a third-party 1GE PCS/PMA module (e.g. 1000BASE-T).

Ethernet flow control

- Supports both classic (802.3x) and class based (802.1Qbb) Ethernet flow control.
- Pause frame generation is controlled through the user I/F Xon/Xoff input sideband signals.
- Pause frames generated using programmable pause quanta values and retransmitted using a configurable retransmission interval.
- Received Pause frames detected by correctly matching the DA, EtherType and Opcode fields.
- Extracted pause quanta values are loaded into decremented counters that control the Xon/Xoff indications sent to the user I/F.

Precision timing

- IEEE 1588v2 support using an optional module.
- Implements Transparent Clock, and assists external software in the support of Master, Slave and Boundary Clock functionality, for the Ethernet, IPv4 and IPv6 encapsulations, in either one-step or two-step mode.
- Assists external software to support other encapsulations no defined by IEEE 1588-2008, such as MPLS or MAC-in-MAC.